CLAIM AMENDMENTS

In the claims:

Please cancel claims 4, 7, 13-14, 16-20, 24, and 26 without prejudice or disclaimer.

Please amend claims 1, 5-6, 8, 11, 15, 21, 25 and 27 as follows.

1. (Currently Amended) A circuit, comprising:

a first switch unit connectable to a first power line, a control line, and a bus line of an assisted Gunning transceiver logic (AGTL)[[-type]] bus, the first switch unit having an impedance that substantially matches the characteristic impedance of the bus line, wherein the first switch unit is to electrically connect the first power line and the bus line when enabled by a control signal received via the control line, wherein the first switch unit is a P-channel transistor; ~~and~~

a second switch unit connectable to a second power line and the bus line, the second switch unit having an impedance different from that of the first switch unit, wherein the second switch unit is to electrically connect **[[**a]] the second power line and the bus line when enabled, the second switch unit to be disabled when the first switch unit is enabled and to be enabled when the first switch unit is disabled; and

a trim circuit coupled to the P-channel transistor, wherein the trim circuit is to compare the impedance of the first switch unit to a reference impedance and to adjust the impedance of the first switch unit to substantially match the reference impedance.

2. (Original) The circuit of claim 1, wherein the second switch unit's impedance is half that of the first switch unit.

3. (Original) The circuit of claim 1, further comprising an amplifier having an input terminal connected to the bus line.

4. (Canceled).

5. (Currently Amended) The circuit of claim [[4]] 1, wherein the first switch unit further comprises a resistor connected in series with the P-channel transistor.

6. (Currently Amended) The circuit of claim [[4]] 5, wherein the resistor is [[a]] an N-well resistor.

7. (Canceled).

8. (Currently Amended) The circuit of claim [[7]] 1, wherein the P-channel transistor comprises a plurality of component P-channel transistors, and wherein the trim circuit to adjust P-channel transistor's effective width-to-length ratio by selectively enabling one or more of the plurality of component P-channel transistors.

9. (Original) The circuit of claim 1, wherein the second switch unit comprises an N-channel transistor.

10. (Original) The circuit of claim 9, wherein the second switch unit further comprises a resistor connected in series with the N-channel transistor.

11. (Currently Amended) A circuit, comprising:

first means for electrically connecting to a first power line and a bus line of an assisted Gunning transceiver logic (AGTL)[[-type]] bus when enabled, the first means having an impedance that substantially matches the bus line's characteristic impedance, wherein the first means is a P-channel transistor and the second means is an N-channel transistor; ~~and~~

second means for electrically connecting a second power line and the bus line when enabled, the second means having an impedance different from that of the first means, wherein the second means is disabled when the first means is enabled and is enabled when the first means is disabled; and

a trim circuit coupled to the P-channel transistor, wherein the trim circuit is to compare the impedance of the first means to a reference impedance and to adjust the impedance of the first means to substantially match the reference impedance.

12. (Original) The circuit of claim 11, wherein the impedance of the second means is half that of the first means.

13. (Canceled).

14. (Canceled).

15. (Currently Amended) The circuit of claim [[13]] 11, wherein the first means further comprises a resistor connected in series with the P-channel transistor.

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Currently Amended) A system, comprising:

an assisted Gunning transceiver logic (AGTL)[[-type]] bus;

a first driver/receiver circuit coupled to one end of a bus line of the AGTL-type bus, the first driver/receiver circuit including:

a first pull-up switch unit to couple a first power line to the bus line, wherein the first pull-up switch unit has an impedance substantially matching the bus line's characteristic impedance, wherein the first pull-up switch unit is a P-channel transistor having one terminal coupled to the first power line;

a first pull-down switch unit coupled to a first ground line and to the bus line, wherein the first pull-down switch unit has an impedance different from that of the first pull-up switch unit; and

a second driver/receiver circuit coupled to another end of the bus line, the second driver/receiver circuit including:

a second pull-up switch unit to electrically connect a second power line to the bus line, the first and second power lines having substantially identical voltage levels, wherein the second pull-up switch unit has an impedance substantially matching that of the first pull-up switch unit, ~~and~~

a second pull-down switch unit coupled to a second ground line and to the bus line, the first and second ground lines having substantially identical voltage levels, wherein the second pull-down switch unit has an impedance substantially matching that of the first pull-down switch unit; and

a trim circuit coupled to the P-channel transistor, wherein the trim circuit is to compare the impedance of the first pull-up switch unit to a reference impedance and to adjust the impedance of the first pull-up switch unit to substantially match that of the reference impedance.

22. (Original) The system of claim 21, wherein the first pull-down switch unit's impedance is half that of the first pull-up switch unit.

23. (Original) The system of claim 21, wherein the first and second driver/receiver circuits each further comprise an amplifier having an input terminal connected to the bus line.

24. (Canceled).

25. (Currently Amended) The system of claim [[24]] 21, wherein the first pull-up switch unit further comprises a resistor connected in series with the P-channel transistor's channel.

26. (Canceled).

27. (Currently Amended) The system of claim [[26]] 21, wherein the P-channel transistor comprises a plurality of component P-channel transistors, and wherein the trim circuit is to adjust P-channel transistor's effective width-to-length ratio by selectively enabling one or more of the plurality of component P-channel transistors.

28. (Original) The system of claim 21, wherein the first pull-down switch unit comprises an N-channel transistor.